

IS61LV256AL

32K x 8 LOW VOLTAGE CMOS STATIC RAM

MARCH 2020

FEATURES

- High-speed access times:
 - 10 ns
- Automatic power-down when chip is deselected
- CMOS low power operation
 - 60 μ W (typical) CMOS standby
 - 65 mW (typical) operating
- TTL compatible interface levels
- Single 3.3V power supply
- Fully static operation: no clock or refresh required
- Three-state outputs
- Lead-free available

DESCRIPTION

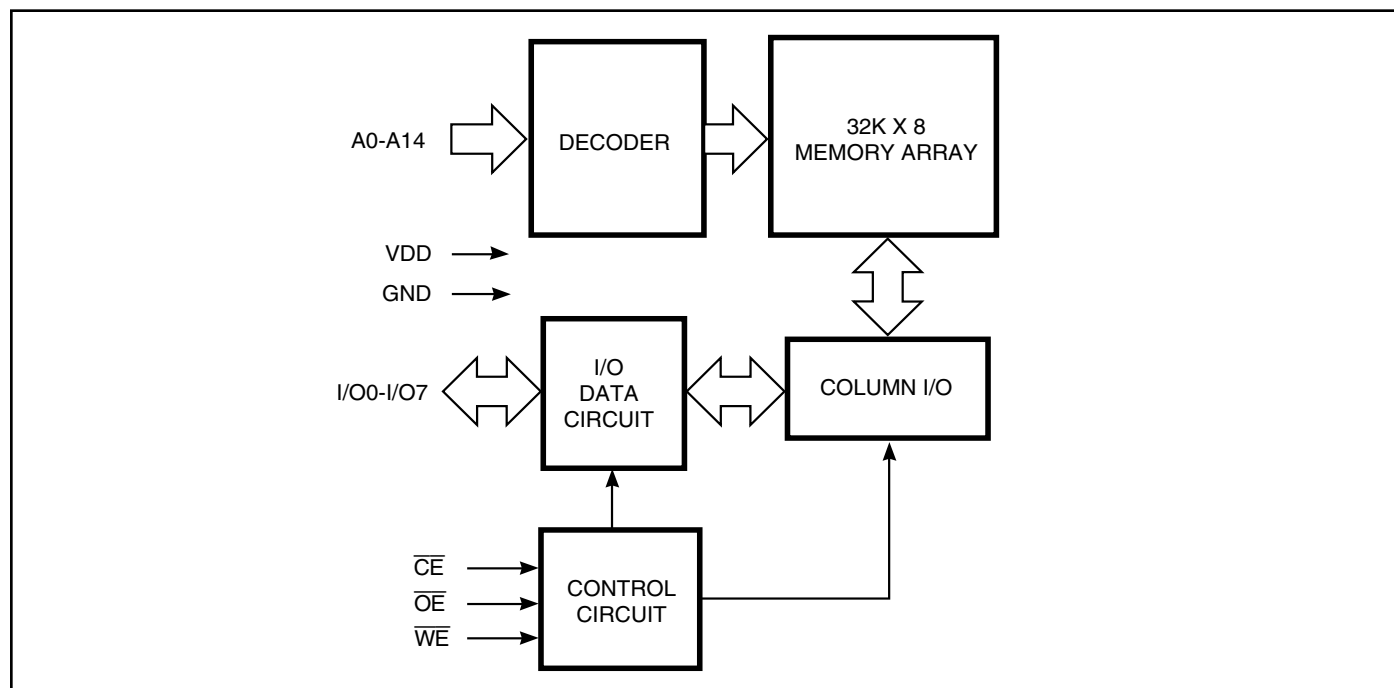
The *ISSI* IS61LV256AL is a very high-speed, low power, 32,768-word by 8-bit static RAM. It is fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields access times as fast as 8 ns maximum.

When $\overline{CE}$ is HIGH (deselected), the device assumes a standby mode at which the power dissipation is reduced to 150 μ W (typical) with CMOS input levels.

Easy memory expansion is provided by using an active LOW Chip Enable ($\overline{CE}$). The active LOW Write Enable ($\overline{WE}$) controls both writing and reading of the memory.

The IS61LV256AL is available in the JEDEC standard 28-pin, 300-mil SOJ and the 450-mil TSOP (Type I) packages.

FUNCTIONAL BLOCK DIAGRAM



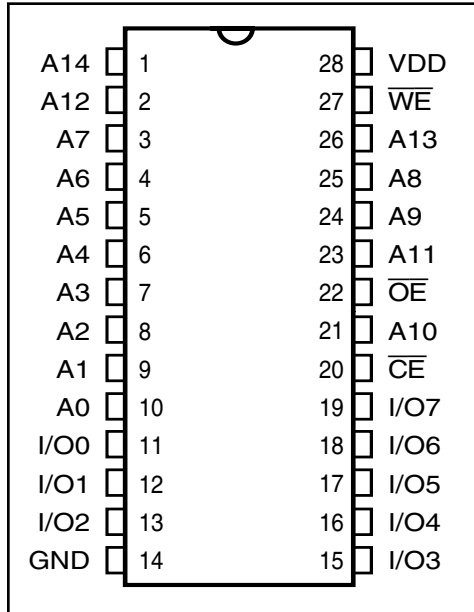
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- b.) the user assume all such risks; and
- c.) potential liability of Integrated Silicon Solution, Inc is adequately protected under the circumstances

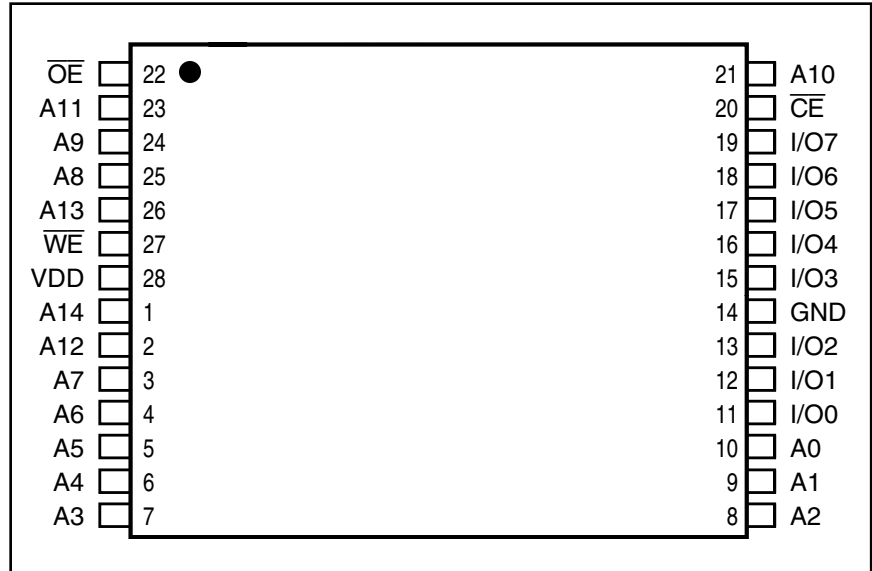
PIN CONFIGURATION

28-Pin SOJ



PIN CONFIGURATION

28-Pin TSOP (Type I)



PIN DESCRIPTIONS

A0-A14	Address Inputs
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
I/O0-I/O7	Input/Output
V _{DD}	Power
GND	Ground

TRUTH TABLE

Mode	$\overline{WE}$	$\overline{CE}$	$\overline{OE}$	I/O Operation	V _{DD} Current
Not Selected (Power-down)	X	H	X	High-Z	I _{SB1} , I _{SB2}
Output Disabled	H	L	H	High-Z	I _{CC}
Read	H	L	L	DOUT	I _{CC}
Write	L	L	X	DIN	I _{CC}

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Parameter	Value	Unit
V _{DD}	Power Supply Voltage Relative to GND	-0.5 to +4.6	V
V _{TERM}	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
T _{STG}	Storage Temperature	-65 to +150	°C
P _D	Power Dissipation	1	W
I _{OUT}	DC Output Current	±20	mA

Notes:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE

Range	Ambient Temperature	Speed (ns)	V _{DD} ⁽¹⁾
Commercial	0°C to +70°C	10	3.3V, +10%, -5%
Industrial	-40°C to +85°C	10	3.3V + 10%, -5%

Note: 1. If operated at 12ns, V_{DD} range is 3.3V $\pm$ 10%.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{DD} = Min., I _{OH} = -2.0 mA	2.4	—	V
V _{OL}	Output LOW Voltage	V _{DD} = Min., I _{OL} = 4.0 mA	—	0.4	V
V _{IH}	Input HIGH Voltage		2.2	V _{DD} + 0.3	V
V _{IL}	Input LOW Voltage ⁽¹⁾		-0.3	0.8	V
I _{LI}	Input Leakage	GND $\leq$ V _{IN} $\leq$ V _{DD}	Com. Ind.	-1 2	μ A
I _{LO}	Output Leakage	GND $\leq$ V _{OUT} $\leq$ V _{DD} , Outputs Disabled	Com. Ind.	-1 2	μ A

Notes:

- V_{IL} (min.) = -0.3V (DC); V_{IL} (min.) = -2.0V (pulse width $\leq$ 2.0 ns).
V_{IH} (max.) = V_{DD} + 0.5V (DC); V_{IH} (max.) = V_{DD} + 2.0V (pulse width $\leq$ 2.0 ns).
- Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.

POWER SUPPLY CHARACTERISTICS⁽¹⁾ (Over Operating Range)

Sym.	Parameter	Test Conditions		-10 ns		Unit
				Min.	Max.	
I _{CC1}	V _{DD} Operating Supply Current	V _{DD} = Max., $\overline{CE}$ = V _{IL}	Com.	—	20	mA
		I _{OUT} = 0 mA, f = 1 MHz	Ind.	—	25	
I _{CC2}	V _{DD} Dynamic Operating Supply Current	V _{DD} = Max., $\overline{CE}$ = V _{IL}	Com.	—	30	mA
		I _{OUT} = 0 mA, f = f _{MAX}	Ind.	—	35	
			typ. ⁽²⁾		20	
I _{SB1}	TTL Standby Current (TTL Inputs)	V _{DD} = Max.,	Com.	—	1	mA
		V _{IN} = V _{IH} or V _{IL} $\overline{CE} \geq V_{IH}$, f = 0	Ind.	—	1	
I _{SB2}	CMOS Standby Current (CMOS Inputs)	V _{DD} = Max.,	Com.	—	40	μA
		$\overline{CE} \geq V_{DD} - 0.2V$,	Ind.	—	50	
		V _{IN} ≥ V _{DD} - 0.2V, or V _{IN} ≤ 0.2V, f = 0	typ. ⁽²⁾		2	

Notes:

- At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.
- Typical values are measured at V_{DD} = 3.3V, T_A = 25°C and not 100% tested.

CAPACITANCE^(1,2)

Symbol	Parameter	Conditions	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	6	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	5	pF

Notes:

- Tested initially and after any design or process changes that may affect these parameters.
- Test conditions: T_A = 25°C, f = 1 MHz, V_{DD} = 3.3V.

READ CYCLE SWITCHING CHARACTERISTICS⁽¹⁾ (Over Operating Range)

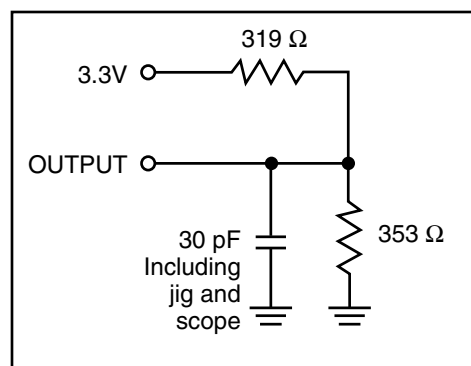
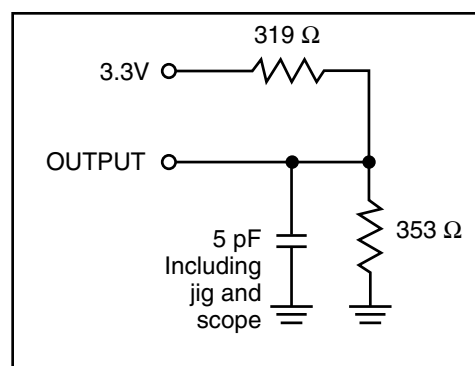
Symbol	Parameter	-10 ns		-12 ns		Unit
		Min.	Max.	Min.	Max.	
t _{RC}	Read Cycle Time	10	—	12	—	ns
t _{AA}	Address Access Time	—	10	—	12	ns
t _{OHA}	Output Hold Time	2	—	2	—	ns
t _{ACE}	$\overline{\text{CE}}$ Access Time	—	10	—	12	ns
t _{DOE}	$\overline{\text{OE}}$ Access Time	—	5	—	5	ns
t _{LZOE} ⁽²⁾	$\overline{\text{OE}}$ to Low-Z Output	0	—	0	—	ns
t _{HZOE} ⁽²⁾	$\overline{\text{OE}}$ to High-Z Output	—	5	—	5	ns
t _{LZCE} ⁽²⁾	$\overline{\text{CE}}$ to Low-Z Output	3	—	3	—	ns
t _{HZCE} ⁽²⁾	$\overline{\text{CE}}$ to High-Z Output	—	5	—	6	ns
t _{PU} ⁽³⁾	$\overline{\text{CE}}$ to Power-Up	0	—	0	—	ns
t _{PD} ⁽³⁾	$\overline{\text{CE}}$ to Power-Down	—	10	—	12	ns

Notes:

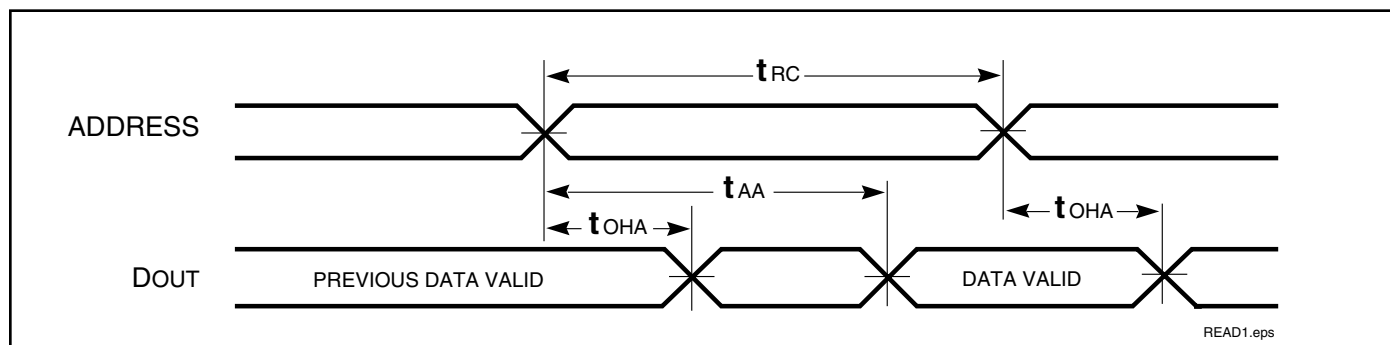
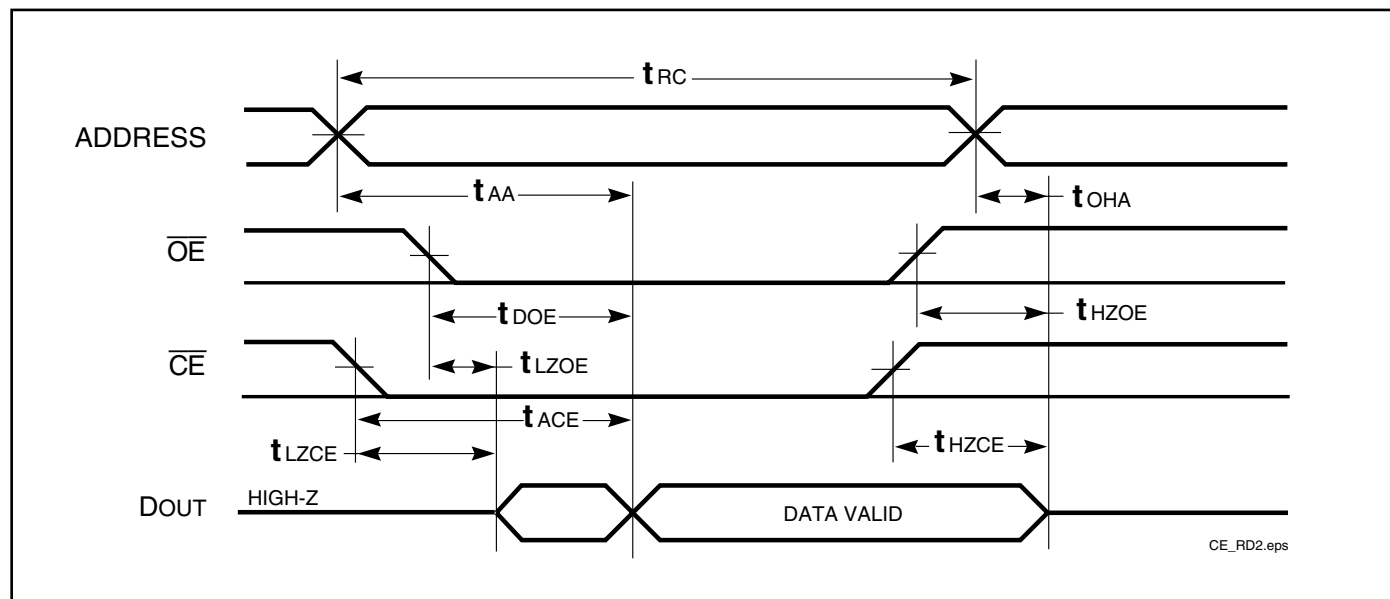
1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ± 200 mV from steady-state voltage. Not 100% tested.
3. Not 100% tested.

AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	3 ns
Input and Output Timing and Reference Levels	1.5V
Output Load	See Figures 1 and 2

AC TEST LOADS**Figure 1.****Figure 2.**

AC WAVEFORMS

READ CYCLE NO. 1^(1,2)READ CYCLE NO. 2^(1,3)

Notes:

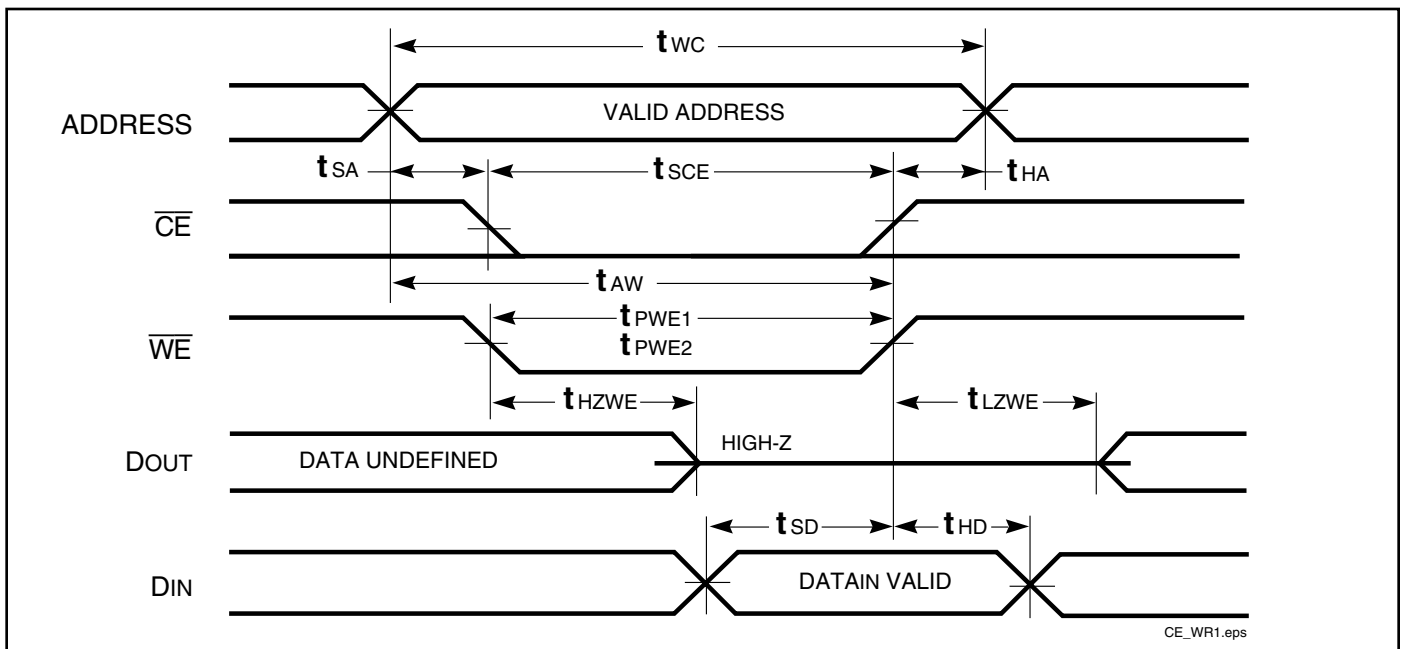
1. $\overline{WE}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL} .
3. Address is valid prior to or coincident with $\overline{CE}$ LOW transitions.

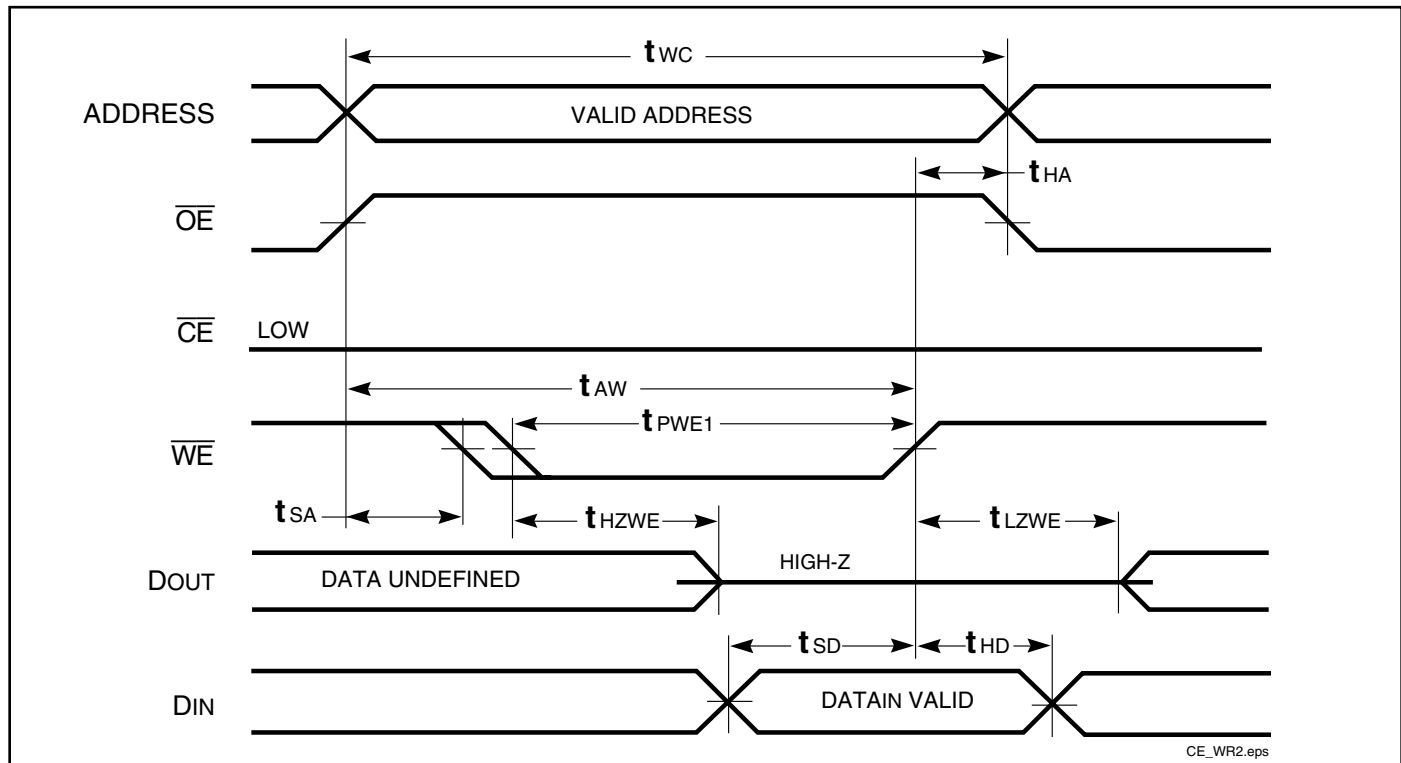
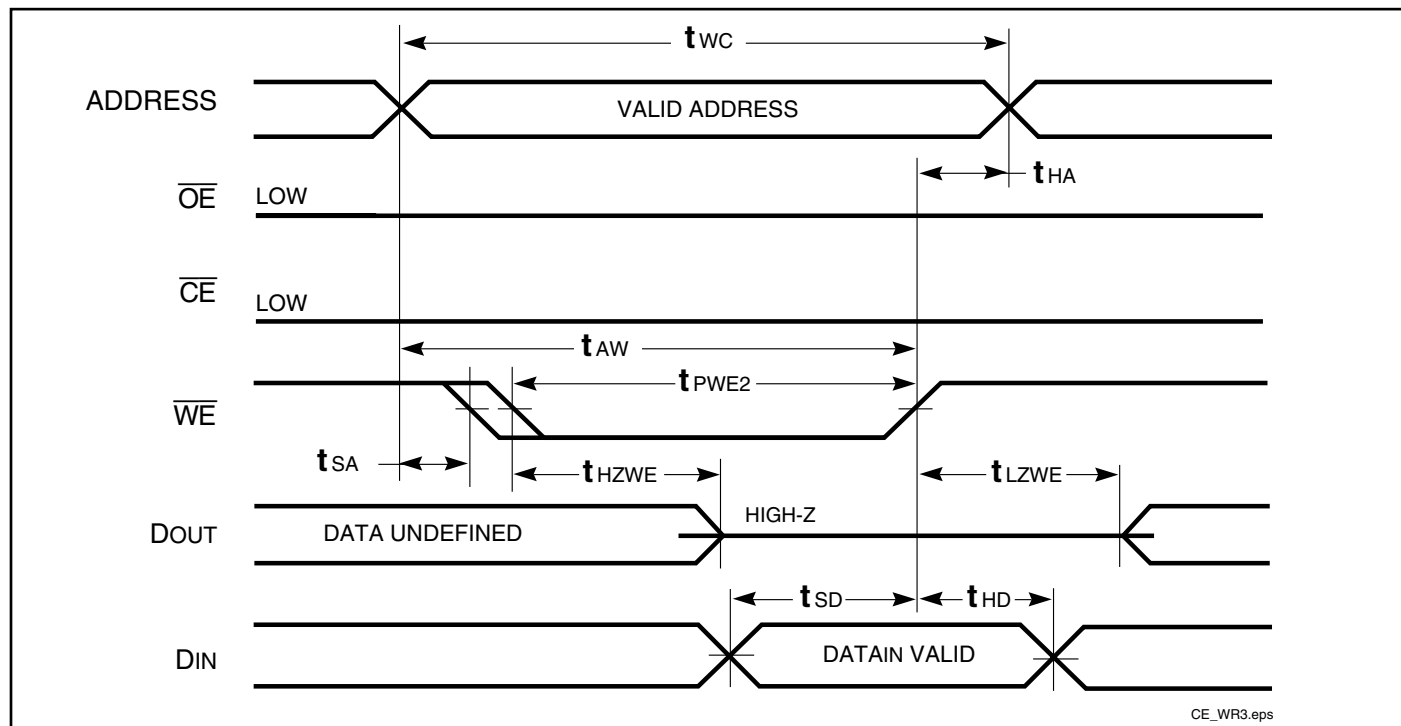
WRITE CYCLE SWITCHING CHARACTERISTICS^(1,2) (Over Operating Range)

Symbol	Parameter	-10 ns		-12 ns		Unit
		Min.	Max.	Min.	Max.	
t _{WC}	Write Cycle Time	10	—	12	—	ns
t _{SCE}	$\overline{CE}$ to Write End	8	—	8	—	ns
t _{AW}	Address Setup Time to Write End	8	—	8	—	ns
t _{HA}	Address Hold from Write End	0	—	0	—	ns
t _{SA}	Address Setup Time	0	—	0	—	ns
t _{PWE1}	$\overline{WE}$ Pulse Width ($\overline{OE}$ HIGH)	7	—	8	—	ns
t _{PWE2}	$\overline{WE}$ Pulse Width ($\overline{OE}$ LOW)	10	—	12	—	ns
t _{SD}	Data Setup to Write End	6.5	—	7	—	ns
t _{HD}	Data Hold from Write End	0	—	0	—	ns
t _{HZWE} ⁽³⁾	$\overline{WE}$ LOW to High-Z Output	—	3.5	—	5	ns
t _{LZWE} ⁽³⁾	$\overline{WE}$ HIGH to Low-Z Output	0	—	0	—	ns

Notes:

1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
3. Tested with the load in Figure 2. Transition is measured ± 500 mV from steady-state voltage. Not 100% tested.

AC WAVEFORMS**WRITE CYCLE NO. 1** ($\overline{CE}$ Controlled, $\overline{OE}$ is HIGH or LOW) ⁽¹⁾

WRITE CYCLE NO. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ is HIGH During Write Cycle) ^(1,2)

WRITE CYCLE NO. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ is LOW During Write Cycle) ⁽¹⁾

Notes:

1. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
2. I/O will assume the High-Z state if $\overline{OE} > V_{IH}$.

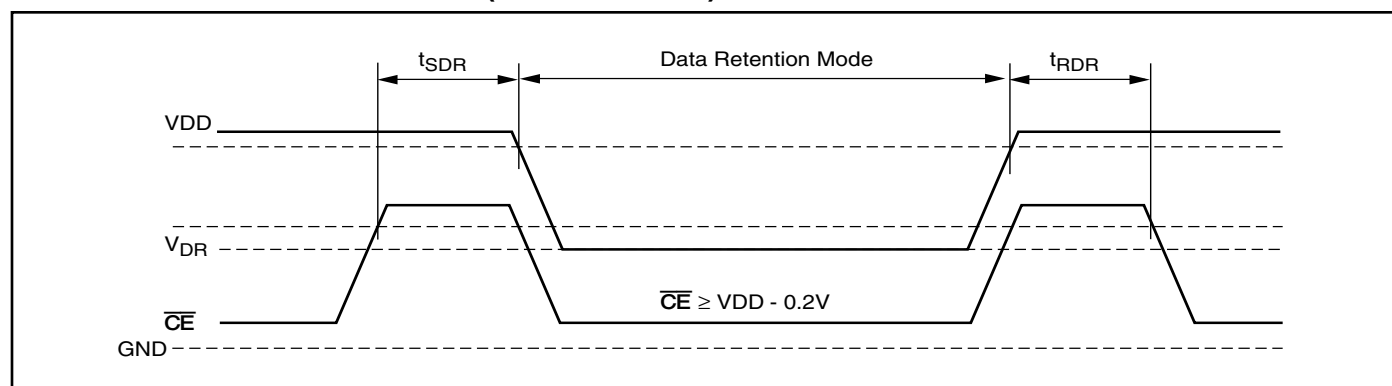
DATA RETENTION SWITCHING CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Typ. ⁽¹⁾	Max.	Unit
V_{DR}	V_{DD} for Data Retention	See Data Retention Waveform	2.0		3.6	V
I_{DR}	Data Retention Current	$V_{DD} = 2.0V$, $\overline{CE} \geq V_{DD} - 0.2V$ $V_{IN} \geq V_{DD} - 0.2V$, or $V_{IN} \leq V_{SS} + 0.2V$	—	2	40	μA
t_{SDR}	Data Retention Setup Time	See Data Retention Waveform	0		—	ns
t_{RDR}	Recovery Time	See Data Retention Waveform	t_{RC}		—	ns

Note:

1. Typical Values are measured at $V_{DD} = 3.3V$, $T_A = 25^\circ C$ and not 100% tested.

DATA RETENTION WAVEFORM ($\overline{CE}$ Controlled)

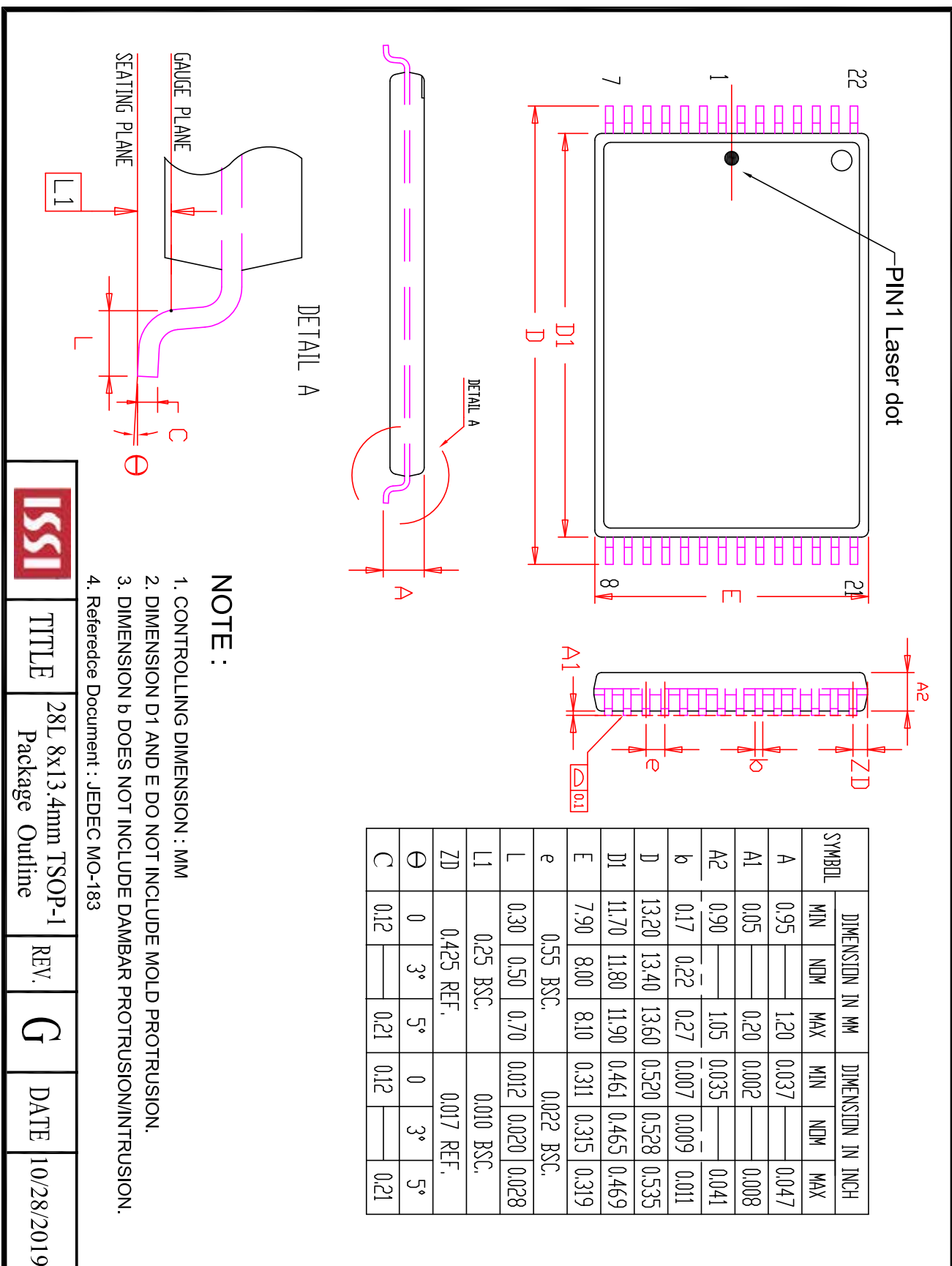


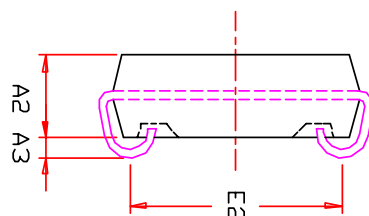
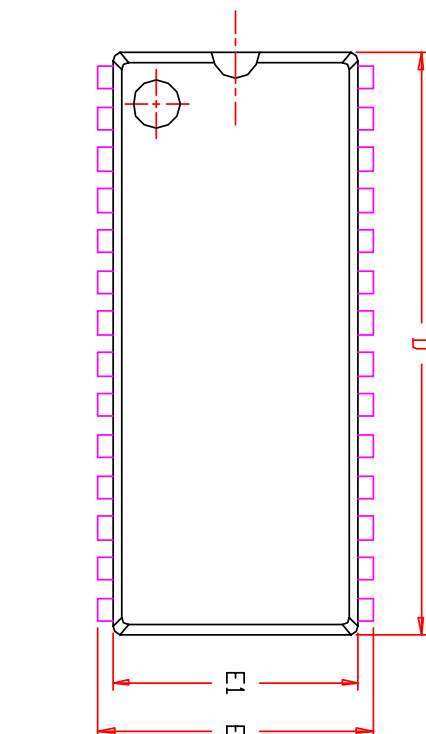
ORDERING INFORMATION**Commercial Range: 0°C to +70°C**

Speed (ns)	Order Part No.	Package
10	IS61LV256AL-10TL	TSOP - Type I, Lead-free
	IS61LV256AL-10JL	300-mil Plastic SOJ, Lead-free

ORDERING INFORMATION**Industrial Range: -40°C to +85°C**

Speed (ns)	Order Part No.	Package
10	IS61LV256AL-10TLI	TSOP - Type I, Lead-free
	IS61LV256AL-10JLI	300-mil Plastic SOJ, Lead-free

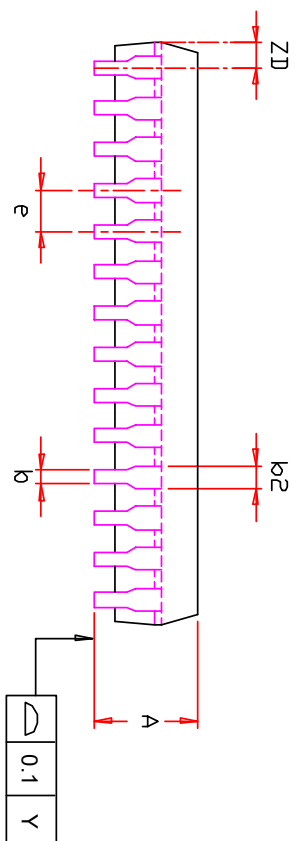




SYMBOL	DIMENSION IN MM		
	MIN.	NOM.	MAX.
A	3.05		3.76
A2	2.41	2.54	2.67
A3	0.64		1.09
b	0.36		0.56
b2	0.66		0.81
D	17.70		18.54
E	8.26	8.56	8.81
E1	7.42		7.75
E2	6.22		7.29
e	1.27	BSC	
ZD	0.95	REF.	
Y		0.1	

NOTE :

1. Controlling dimension : mm
2. Dimension D1 adn E do not include mold protrusion .
3. Dimension b2 does not include dambar protrusion/intrusion.
4. Formed leads shall be planar with respect to one another within 0.1mm at the seating plane after final test.



ISSI		TITLE	REV.	DATE
28L 300mil SOI		Package Outline	C	07/05/2006